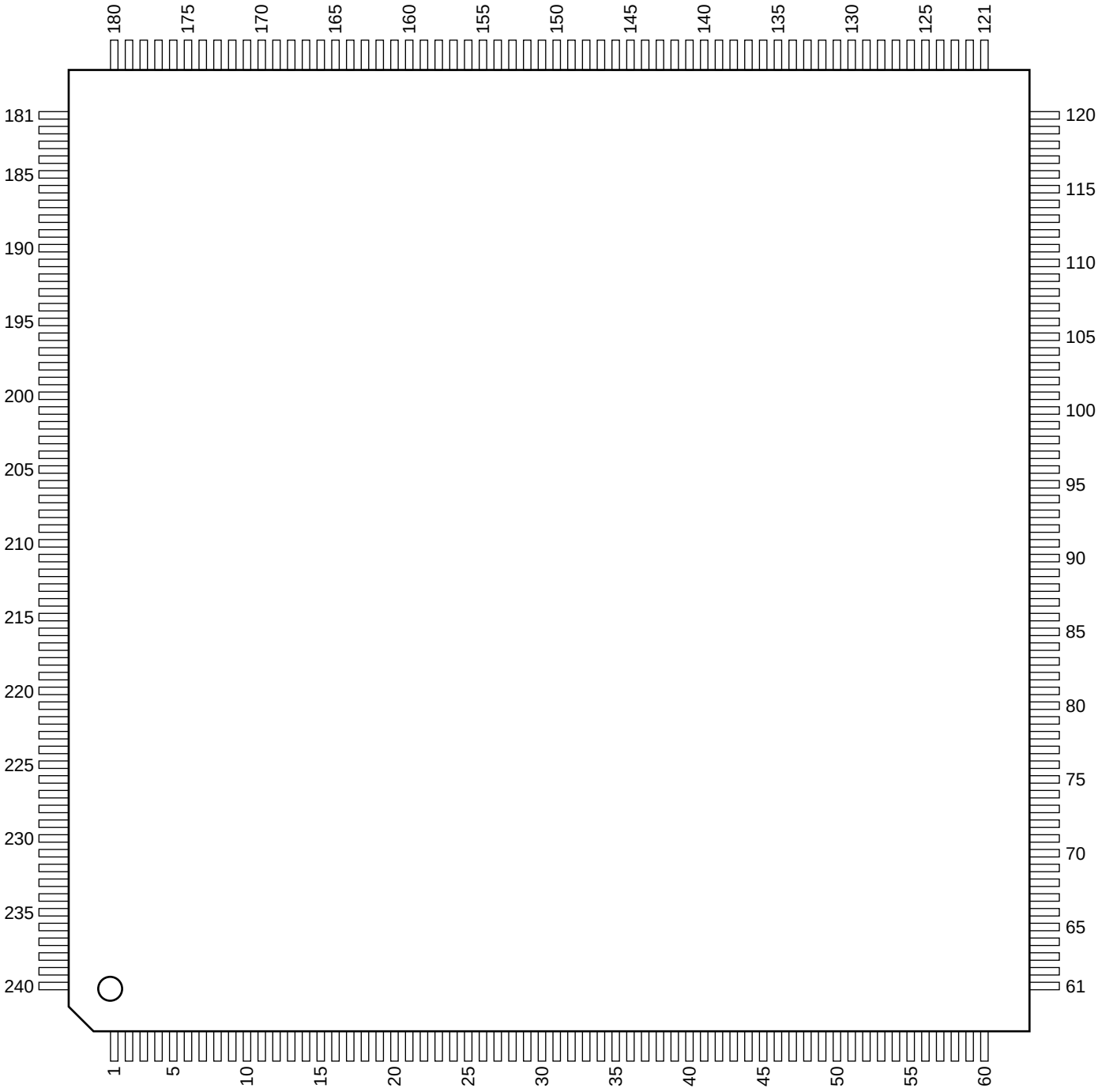
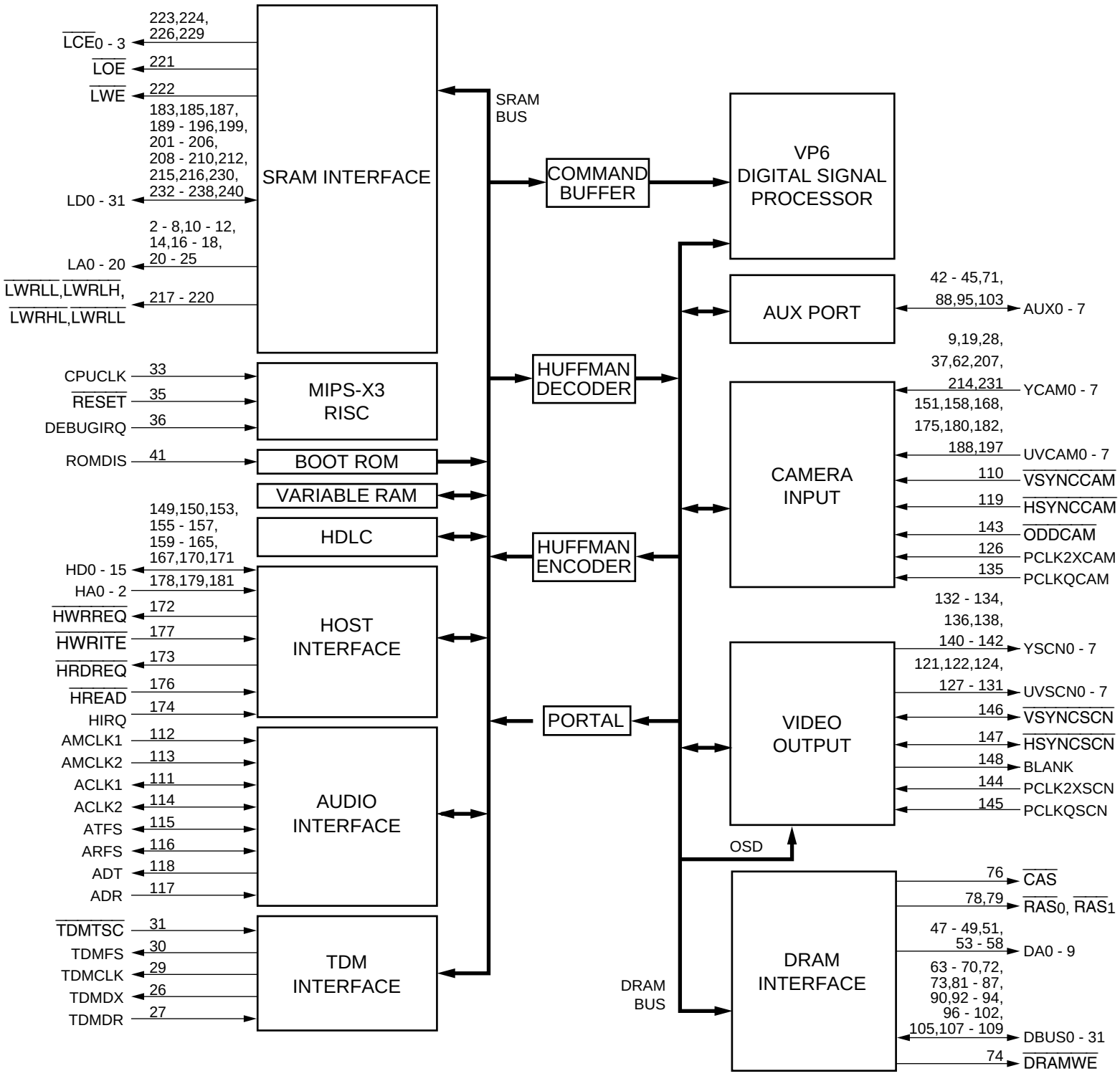
VIDEO COMMUNICATION PROCESSOR

–TOP VIEW–



PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	VDD_IO	51	O	DA3	101	I/O	DBUS13	151	I	UVCAM0
2	O	LA19	52	—	VCC	102	I/O	DBUS29	152	—	GND
3	O	LA18	53	O	DA4	103	I/O	AUX7	153	I/O	HD2
4	O	LA17	54	O	DA5	104	—	GND	154	—	VCC
5	O	LA16	55	O	DA6	105	I/O	DBUS14	155	I/O	HD3
6	O	LA15	56	O	DA7	106	—	VCC	156	I/O	HD4
7	O	LA14	57	O	DA8	107	I/O	DBUS30	157	I/O	HD5
8	O	LA13	58	O	DA9	108	I/O	DBUS15	158	I	UVCAM1
9	I	YCAM3	59	—	VCC	109	I/O	DBUS31	159	I/O	HD6
10	O	LA12	60	—	GND_IO	110	I	$\overline{\text{VSYNCCAM}}$	160	I/O	HD7
11	O	LA11	61	—	VDD_IO	111	I/O	ACLK1	161	I/O	HD8
12	O	LA10	62	I	YCAM7	112	I	AMCLK1	162	I/O	HD9
13	—	GND_IO	63	I/O	DBUS0	113	I	AMCLK2	163	I/O	HD10
14	O	LA9	64	I/O	DBUS16	114	I/O	ACLK2	164	I/O	HD11
15	—	VDD_IO	65	I/O	DBUS1	115	I/O	ATFS	165	I/O	HD12
16	O	LA8	66	I/O	DBUS17	116	I/O	ARFS	166	—	GND
17	O	LA7	67	I/O	DBUS2	117	I	ADR	167	I/O	HD13
18	O	LA6	68	I/O	DBUS18	118	O	ADT	168	I	UVCAM2
19	I	YCAM4	69	I/O	DBUS3	119	I	$\overline{\text{HSYNCCAM}}$	169	—	VCC
20	O	LA5	70	I/O	DBUS19	120	I	TEST	170	I/O	HD14
21	O	LA4	71	I/O	AUX4	121	O	UVSCN0	171	I/O	HD15
22	O	LA3	72	I/O	DBUS4	122	O	UVSCN1	172	O	$\overline{\text{HWRREQ}}$
23	O	LA2	73	I/O	DBUS20	123	—	GND_IO	173	O	$\overline{\text{HRDREQ}}$
24	O	LA1	74	O	$\overline{\text{DRAMWE}}$	124	O	UVSCN2	174	O	HIRQ
25	O	LA0	75	—	GND_IO	125	—	VDD_IO	175	I	UVCAM3
26	O	TDMDX	76	O	$\overline{\text{CAS}}$	126	I	PCLK2XCAM	176	I	$\overline{\text{HREAD}}$
27	I	TDMDR	77	—	GND_IO	127	O	UVSCN3	177	I	$\overline{\text{HWRITE}}$
28	I	YCAM5	78	O	$\overline{\text{RAS1}}$	128	O	UVSCN4	178	I	HA0
29	I	TDMCLK	79	O	$\overline{\text{RAS0}}$	129	O	UVSCN5	179	I	HA1
30	I	TDMFS	80	—	GND	130	O	UVSCN6	180	I	UVCAM4
31	O	$\overline{\text{TDMTSC}}$	81	I/O	DBUS5	131	O	UVSCN7	181	I	HA2
32	—	GND	82	I/O	DBUS21	132	O	YSCN0	182	I	UVCAM5
33	I	CPUCLK	83	I/O	DBUS6	133	O	YSCN1	183	I/O	LD0
34	—	VCC	84	I/O	DBUS22	134	O	YSCN2	184	—	GND_IO
35	I	$\overline{\text{RESET}}$	85	I/O	DBUS7	135	I	PCLKQCAM	185	I/O	LD8
36	I	DEBUGIRQ	86	I/O	DBUS23	136	O	YSCN3	186	—	VDD_IO
37	I	YCAM6	87	I/O	DBUS8	137	—	GND_IO	187	I/O	LD16
38	I	TRIMODE	88	I/O	AUX5	138	O	YSCN4	188	I	UVCAM6
39	I	TEST	89	—	GND	139	—	VDD_IO	189	I/O	LD24
40	I	TEST	90	I/O	DBUS24	140	O	YSCN5	190	I/O	LD1
41	I	ROMDIS	91	—	VCC	141	O	YSCN6	191	I/O	LD9
42	I/O	AUX0	92	I/O	DBUS9	142	O	YSCN7	192	I/O	LD17
43	I/O	AUX1	93	I/O	DBUS25	143	I	$\overline{\text{ODDCAM}}$	193	I/O	LD25
44	I/O	AUX2	94	I/O	DBUS10	144	I	PCLK2XSCN	194	I/O	LD2
45	I/O	AUX3	95	I/O	AUX6	145	I	PCLKQSCN	195	I/O	LD10
46	—	GND	96	I/O	DBUS26	146	I/O	$\overline{\text{VSYNCSCN}}$	196	I/O	LD18
47	O	DA0	97	I/O	DBUS11	147	I/O	$\overline{\text{HSYNCSCN}}$	197	I	UVCAM7
48	O	DA1	98	I/O	DBUS27	148	O	BLANK	198	—	GND
49	O	DA2	99	I/O	DBUS12	149	I/O	HD0	199	I/O	LD26
50	—	GND	100	I/O	DBUS28	150	I/O	HD1	200	—	VDD_IO

PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
201	I/O	LD3	211	—	GND	221	O	$\overline{LOE}$	231	I	YCAM2
202	I/O	LD11	212	I/O	LD13	222	O	$\overline{LWE}$	232	I/O	LD14
203	I/O	LD19	213	—	VCC	223	O	$\overline{LCE0}$	233	I/O	LD22
204	I/O	LD27	214	I	YCAM1	224	O	$\overline{LCE1}$	234	I/O	LD30
205	I/O	LD4	215	I/O	LD21	225	—	GND	235	I/O	LD7
206	I/O	LD12	216	I/O	LD29	226	O	$\overline{LCE2}$	236	I/O	LD15
207	I	YCAM0	217	O	$\overline{LWRLL}$	227	—	VCC	237	I/O	LD23
208	I/O	LD20	218	O	$\overline{LWRLH}$	228	—	VDD_IO	238	I/O	LD31
209	I/O	LD28	219	O	$\overline{LWRHL}$	229	O	$\overline{LCE3}$	239	—	GND_IO
210	I/O	LD5	220	O	$\overline{LWRHH}$	230	I/O	LD6	240	O	LA20



INPUTS

ADR	:	AUDIO DATA RECEIVE
AMCLK1, AMCLK2	:	FAIN INPUT CLOCK
CPUCLK	:	SYSTEM CLOCK
DEBUGIRQ	:	SYSTEM DEBUG IRQ
HA0 - 2	:	HOST ADDRESS BUS
$\overline{\text{HREAD}}$	:	HOST READ STROBE
$\overline{\text{HSYNCCAM}}$	:	VIDEO CAMERA HORIZONTAL START
$\overline{\text{HSYNCSCN}}$	:	SCREEN HORIZONTAL START
$\overline{\text{HWRITE}}$	:	HOST WRITE STROBE
$\overline{\text{ODDCAM}}$	:	VIDEO CAMERA ODD/EVEN FIELD
PCLKQCAM	:	VIDEO CAMER PIXEL CLOCK QUALIFIER
PCLKQSCN	:	SCREEN PIXEL CLOCK QUALIFIER
PCLK2XSCN	:	SCREEN 2X PIXEL CLOCK
PCLK2XCAM	:	VIDEO CAMERA 2X PIXEL CLOCK
$\overline{\text{RESET}}$	:	SYSTEM RESET
ROMDIS	:	DESABLE THE INTERNAL BOOT ROM
TDMCLK	:	TDM CLOCK
TDMDR	:	TDM DATA RECEIVE
TDMFS	:	TDM FRAME SYNC
TEST	:	TEST PIN, MUST BE PULLED LOW
TRIMODE	:	3-STATE OUTPUT DRIVERS
UVCAM0 - 7	:	VIDEO CAMERA UV DATA
$\overline{\text{VSYNCCAM}}$	:	VIDEO CAMERA VERTICAL START
YCAM0 - 7	:	VIDEO CAMERA Y DATA

OUTPUTS

ADT	:	AUDIO DATA TRANSMIT
BLANK	:	SCREEN BLANKING
$\overline{\text{CAS}}$	:	COLUMN ADDRESS STROBE
DA0 - 9	:	DRAM MUITIPLEXED ADDRESS BUS
$\overline{\text{DRAMWE}}$	:	DRAM WRITE ENABLE
HIRQ	:	VCP TO HOST IRQ
$\overline{\text{HRDREQ}}$	:	HOST READ REQUEST
$\overline{\text{HWRREQ}}$	:	HOST WRITE REQUEST
LA0 - 20	:	RISC ADDRESS BUS
$\overline{\text{LCE}}$0 - 3	:	CHIP ENABLES FOR 4-SRAM BANKS
$\overline{\text{LOE}}$	:	SRAM/ROM OUTPUT ENABLE
$\overline{\text{LWE}}$	:	WRITE ENABLE FOR 16-BIT WIDE SRAM
$\overline{\text{LWRLL}}$, $\overline{\text{LWRLH}}$, $\overline{\text{LWRHL}}$, $\overline{\text{LWRHH}}$	:	BYTE WRITE ENABLES FOR 8-BIT WIDE SRAM
$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$	:	ROW ADDRESS STROBE FOR BANKS
TDMDX	:	TDM DATA TRANSMIT
$\overline{\text{TDMTSC}}$	:	TDM 3-STATE CONTROL
UVSCN0 - 7	:	SCREEN UV DATA
YSCN0 - 7	:	SCREEN Y DATA

INPUTS/OUTPUTS

ACLK1, ACLK2	:	AUDIO CLOCK
ARFS	:	RECEIVE FRAME SYNC
ATFS	:	TRANSMIT FRAME SYNC
AUX0 -7	:	SYSTEM AUXILIARY CONTROL LINES
DBUS0 - 31	:	DRAM DATA BUS
HD0 - 15	:	HOST DATA BUS
$\overline{\text{HSYNCSCN}}$	:	SCREEN HORIZONTAL START
LD0 - 31	:	RISC DATA BUS
$\overline{\text{VSYNCSCN}}$	:	SCREEN VERTICAL START